WHAT IS CLAIMED IS:

1. An information processing apparatus including processor means for executing an operation and storage means for storing an instruction or data for said processor means to execute the operation, the information processing apparatus comprising:

a plurality of transfer means for transferring said instruction or data between said processor means and said storage means; and

at least one address translation means for translating a virtual address designated by said processor means into a physical address of said storage means,

wherein each of said transfer means includes an independent virtual address space including addresses, which is mutually overlapping with virtual address spaces of the other transfer means; and

said address translation means translates said virtual address space of said transfer means into a single physical address space.

2. The information processing apparatus according to claim 1, wherein:

said transfer means includes an instruction bus for transferring said instruction and a data bus for transferring said data; and

a difference between a virtual address of an instruction accompanying an access to said transfer means and a virtual address of data accessed by said instruction is equal to or shorter than a distance which can be directly designated as a relative address by an operand of the instruction.

3. The information processing apparatus according to claim 1, further comprising:

a cache, provided for each of said transfer means, said cache using said virtual address as a tag.

4. The information processing apparatus according to claim 3,

wherein said virtual address space includes virtual addresses in such a manner that a border between a virtual address of said instruction and a virtual address of said data becomes a line border of said cache.

5. The information processing apparatus according to claim 1, further comprising:

a cache for making a distinction between a plurality of said transfer means and identifying cache data.

6. The information processing apparatus according to claim 5,

wherein said virtual address space includes virtual addresses in such a manner that a border between a virtual address of said instruction and a virtual address of said data becomes a line border of said cache.

7. The information processing apparatus according to claim 1,

wherein if a translation unit of an address to be translated by said address translation means contains both a virtual address of said instruction and a virtual address of said data, data included in said translation unit is only

constant data.

8. The information processing apparatus according to claim 1,

wherein said address translation means translates said virtual address space of said transfer means into said single physical address space having mutually non-overlapping addresses.

9. The information processing apparatus according to claim 1,

wherein said storage means includes a write inhibited area and a write permitted area; and

virtual addresses of both said write inhibited area and said write permitted area are disposed in a virtual address space in a range that can be directly designated as a relative address by an operand of an instruction accompanying an access to said storage means.

10. The information processing apparatus according to claim 1,

wherein said storage means includes at least one input/output (I/O) register; and

a difference between a virtual address of said instruction accompanying an access to said I/O register and a virtual address representative of said I/O register is equal to or shorter than a distance that can be directly designated as a relative address by an operand of said instruction.

11. The information processing apparatus according to claim 10,

wherein a virtual address representative of a same I/O register is divided and disposed in a plurality of areas of said virtual address space.

12. The information processing apparatus according to claim 1,

wherein said address translation means translates upper n bits of said virtual address of (n + m) bits, and at least one bit or more of the translated upper n bits is exchanged with at least one or more bits of the remaining m bits, thereby translating said virtual address into said physical address.

13. The information processing apparatus according to claim 1,

wherein said address translation means translates upper n bits of said virtual address of (n + m) bits, and at least one bit or more of the remaining lower m bits is exchanged with another one bit or more of the remaining lower m bits, thereby translating said virtual address into said physical address.

14. An information processing method for an information processing apparatus, the information processing apparatus including:

processor means for executing an operation;

storage means for storing an instruction or data for said processor means to execute the operation;

a plurality of transfer means for transferring said instruction or data between said processor means and said storage means; and

at least one address translation means for translating

a virtual address designated by said processor means into a physical address of said storage means,

wherein each of said transfer means includes an independent virtual address space including addresses, which is mutually overlapping with virtual address spaces of the other transfer means; and

said address translation means includes a translation step of translating said virtual address space of said transfer means into a single physical address space.

15. The information processing method according to claim 14, further comprising the step of:

assigning virtual addresses in such a manner that said independent virtual address space of said transfer means includes addresses mutually overlapped with virtual address spaces of said other transfer means.

16. A storage medium storing a computer readable program for an information processing apparatus, the information processing apparatus comprising:

processor means for executing an operation;

storage means for storing an instruction or data necessary for said processor means to execute the operation;

a plurality of transfer means for transferring said instruction or data between said processor means and said storage means; and

at least one address translation means for translating a virtual address designated by said processor means into a physical address of said storage means,

wherein each of said transfer means includes an independent virtual address space including addresses, which

is mutually overlapping with virtual address spaces of the other transfer means; and

said address translation means includes a translation step of translating said virtual address space of said transfer means into a single physical address space.

17. The storage medium according to claim 16, further comprising the step of:

assigning virtual addresses in such a manner that said independent virtual address space of said transfer means includes addresses mutually overlapped with virtual address spaces of said other transfer means.

18. A program for causing an information processing apparatus to execute, the information processing apparatus including:

processor means for executing an operation;

storage means for storing an instruction or data necessary for said processor means to execute the operation;

a plurality of transfer means for transferring said instruction or data between said processor means and said storage means; and

at least one address translation means for translating a virtual address designated by said processor means into a physical address of said storage means,

wherein each of said transfer means includes an independent virtual address space including addresses, which is mutually overlapping with virtual address spaces of the other transfer means; and

said address translation means includes a translation step of translating said virtual address space of said transfer means into a single physical address space.

19. The program according to claim 18, further comprising the step of:

assigning virtual addresses in such a manner that said independent virtual address space of said transfer means includes addresses mutually overlapped with virtual address spaces of said other transfer means.

20. An imaging apparatus comprising:

imaging means for taking an image of an object;

encoding means for encoding image data of the object taken with said imaging means;

processor means for executing an operation of designating an instruction or data for said encoding means to encode said image data; and

storage means for storing said instruction or data for said processor means to execute an operation,

wherein the imaging apparatus further comprises:

a plurality of transfer means for transferring said instruction or data between said processor means and said storage means; and

at least one address translation means for translating a virtual address designated by said processor means into a physical address of said storage means,

wherein each of said transfer means includes an independent virtual address space including addresses, which is mutually overlapping with virtual address spaces of the other transfer means;

said address translation means translates said virtual address space of said transfer means into a single physical address space; and

said encoding means encodes said image data in accordance with said instruction or data in said storage means corresponding to an address designated by said processor means and translated by said address translation means.

21. An information processing apparatus including a processor for executing an operation and a storage for storing an instruction or data for said processor to execute the operation, the information processing apparatus comprising:

a plurality of transfer sections for transferring said instruction or data between said processor and said storage; and

at least one address translator for translating a virtual address designated by said processor into a physical address of said storage,

wherein each of said transfer section includes an independent virtual address space including addresses, which is mutually overlapping with virtual address spaces of the other transfer section; and

said address translator translates said virtual address space of said transfer section into a single physical address space.

22. An imaging apparatus comprising:

an imaging section for taking an image of an object;

an encoder for encoding image data of the object taken with said imaging section;

a processor for executing an operation of designating an instruction or data for said encoder to encode said image data; and

a storage for storing said instruction or data for said

processor to execute an operation,

wherein the imaging apparatus further comprises:

a plurality of transfer sections for transferring said instruction or data between said processor and said storage; and

at least one address translator for translating a virtual address designated by said processor into a physical address of said storage,

wherein each of said transfer section includes an independent virtual address space including addresses, which is mutually overlapping with virtual address spaces of the other transfer section;

said address translator translates said virtual address space of said transfer section into a single physical address space; and

said encoder encodes said image data in accordance with said instruction or data in said storage corresponding to an address designated by said processor and translated by said address translation section.